Claim Amendments

Claims 1, 3, 4, 17, 18, and 21 have been amended. Claims 2, 5-16, 19, and 20 are unchanged. The following listing of claims replaces all previous versions of the claims in the application.

Listing of Claims

1. (currently amended) A method for using a logic design system to implement a logic design in a programmable logic device, comprising:

using the logic design system to allow a logic designer to specify a desired logic design; and

generating configuration data for the programmable logic device using the logic design system that takes into account ~~of~~ power consumption due to gate leakage effects.

2. (original) The method defined in claim 1 wherein there are signals on the programmable logic device, the method further comprising using the logic design system to gather information on the signals from the logic designer.

3. (currently amended) The method defined in claim 1 further comprising using the logic design system to produce

configuration data that helps to reduce power consumption by the programmable logic device due to gate leakage effects by taking into account ~~of~~ transistor stacking effects in logic gates on the programmable logic device.

4. (currently amended) The method defined in claim 1 wherein the programmable logic device includes logic gates having stacks of transistors, the method further comprising using the logic design system to produce configuration data for the programmable logic device that configures the programmable logic device to route signals on the programmable logic device to positions within the stacks based on ~~the~~ amounts that the signals are expected to be high or low.

5. (original) The method defined in claim 1 wherein there are signals on the programmable logic device, the method further comprising analyzing the logic design with the logic design system to automatically generate information on the signals.

6. (original) The method defined in claim 1 wherein the programmable logic device includes logic gates containing stacks of transistors and wherein there are signals on the programmable logic device, the method further comprising using

the logic design system to produce configuration data that helps to reduce power consumption due to gate leakage effects in the programmable logic device by configuring the programmable logic device so that the signals that are handled by transistors that are higher in the stacks are more likely to be high than signals that are handled by transistors that are lower in the stacks.

7. (original) A method for using a logic design system to minimize power consumption in a programmable logic device, comprising:

using the logic design system to receive a desired logic design from a logic designer; and

producing configuration data for the programmable logic device with the logic design system that, when programmed into the programmable logic device, implements the desired logic design in the programmable logic device while routing signals on the programmable logic device to reduce power consumption due to gate leakage effects.

8. (original) The method defined in claim 7 wherein the programmable logic device includes logic gates having stacks of transistors with transistor gates and wherein producing the configuration data comprises producing configuration data that ensures that signals that are more likely to be high are routed

to the transistor gates of the transistors higher in the stacks and that signals that are less likely to be high are routed to the transistor gates of the transistors lower in the stacks.

9. (original) The method defined in claim 7 further comprising using the logic design system to receive a plurality of logic design constraints from the logic designer, wherein one of the constraints involves minimizing power consumption due to gate leakage effects and wherein producing the configuration data comprises producing configuration data that balances the plurality of constraints.

10. (original) The method defined in claim 7 wherein the programmable logic device includes at least one logic gate having a stack of transistors with transistor gates, wherein a first one of the transistors is higher in the stack than a second one of the transistors, and wherein first and second signals are received by the transistor gates, wherein the first signal is high more often than the second signal, and wherein producing the configuration data comprises producing configuration data that, when programmed into the programmable logic device, causes the first signal to be received by the first transistor gate and the second signal to be received by

the second transistor gate to reduce power consumption due to gate leakage.

11. (original) The method defined in claim 10 further comprising using the logic design system to receive information on the first and second signals from the logic designer, wherein the information on the first and second signals includes information that the first signal is high more often that the second signal.

12. (original) The method defined in claim 10 further comprising using the logic design system to automatically analyze the logic design to produce information that the first signal is high more often than the second signal.

13. (original) The method defined in claim 7 further comprising:

using the logic design system to gather signal type information from the logic designer; and

using the signal type information to determine how to route signals on the programmable logic device to minimize power consumption due to gate leakage.

14. (original) A logic design system comprising computing equipment configured to:

receive a logic design from a logic designer; and

use placement and routing tools including a gate leakage optimizer tool implemented on the computing equipment to produce configuration data for a programmable logic device, wherein the configuration data, when programmed into the programmable logic device, causes signals to be routed to transistor gates on the programmable logic device based on the likelihood of those signals to be high or low to reduce power consumption due to gate leakage.

15. (original) The logic design system defined in claim 14, wherein the computing equipment comprises at least one personal computer and wherein, the computing equipment is further configured to:

receive information on logic design constraints from the logic designer, wherein the constraints include a minimum desired clock speed; and

satisfy the minimum desired clock speed constraint while reducing the power consumption due to gate leakage by producing the configuration data that routes signals

to transistor gates based on the likelihood of those signals to be high or low.

16. (original) The logic design system defined in claim 14, wherein the computing equipment is further configured to perform logical synthesis and optimization on the logic design.

17. (currently amended) A method for ~~generating~~ using a logic design system to generate configuration data for a programmable logic device to minimize power consumption due to gate leakage in transistors in logic gate stacks on the programmable logic device when the programmable logic device is operated after having been programmed with the configuration data, wherein some transistors are more likely to produce lower gate leakage than other transistors when high voltages are applied to their gates due to their positions in the stacks, the method comprising:

receiving a logic design from a logic designer; and

producing configuration data to implement the logic design in the programmable logic device while ensuring that at least some signals that have a high likelihood of being high are routed to those transistors that are more likely to

produce the lower gate leakage than the other transistors when high voltages are applied to their gates.

18. (currently amended) The method defined in claim 17 further comprising using the logic design system to receive information from the logic designer on ~~the~~ an expected fraction of a given signal's operation that the signal is to be high.

19. (original) The method defined in claim 18 further comprising using the information on the expected fraction of the given signal's operation that the signal is to be high to produce configuration data that lowers power consumption by the programmable logic device due to gate leakage.

20. (original) The method defined in claim 17 further comprising:

using the logic design system to automatically analyze the logic design to determine which signals are likely to be high and which signals are likely to be low; and

producing configuration data that routes at least some of the signals that are likely to be high to the transistors that are likely to produce low gate leakage when high signals are applied to their gates.

21. (currently amended) A computer-readable medium having instructions for causing computing equipment to execute a method comprising:

producing configuration data for a programmable logic device that takes into account ~~of~~ gate leakage effects to minimize gate leakage power consumption by the programmable logic device.